AMENDMENTS TO CLAIMS

Please amend the claims as shown in the following listing of claims which will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1-21. (Canceled.)

22.   A DDR memory device having an interface, wherein the interface comprises a general command interface configured to receive a general command.

23.   A DDR memory device according to claim 22, wherein the general command interface is configured to receive a general command from a supplementary command bus.

24.   A DDR memory device according to claim 23, wherein the general command is a PRECHARGE command.

25.   A DDR memory device according to claim 23, wherein the general command is a PRE-ACCESS command.

26.   A DDR memory device according to claim 22, wherein the DDR memory device comprises more than one memory bank, and the interface further comprises a general bank select interface configured to receive bank address information associated with the general command.

27.   A DDR memory device according to claim 22, further comprising a main command interface configured to receive a main command from a main command bus.

28.   A SDRAM memory device having an interface, wherein the interface comprises a general command interface configured to receive a general command.

29.   A SDRAM memory device according to claim 28, wherein the general command interface is configured to receive the general command from a supplementary command bus.

30. A SDRAM memory device according to claim 29, wherein the general command is a PRECHARGE command.

31. A SDRAM memory device according to claim 29, wherein the general command is a PRE-ACCESS command.

32. A SDRAM memory device according to claim 28, wherein the SDRAM memory device comprises more than one memory bank, and the interface further comprises a general bank select interface configured to receive bank address information associated with the general command.

33. A SDRAM memory device according to claim 28, further comprising a main command interface configured to receive a main command from a main command bus.

34. A memory device comprising:

an interface that is configured to communicate with a supplementary control bus, wherein the supplementary control bus comprises: a supplementary command bus, a supplementary chip select bus, and a supplementary bank select bus;

wherein the supplementary command bus is a one-bit bus that is configured to communicate a supplementary command bit, and wherein assertion of the supplementary command bit causes execution of a PRECHARGE command on a first memory bank that is identified by signals from the supplementary chip select bus and the supplementary bank select bus.

35. A memory device according to claim 34 further comprising an interface that is configured to communicate with a main control bus, wherein the main control bus is configured to assert at least one of ACTIVE, READ and WRITE commands in conjunction with an address bus.

36.	A memory device according to claim 35 wherein the memory device is configured to assert an ACTIVE command, via the main control bus, on a second memory bank, and wherein the memory device is further configured to concurrently assert, via the supplementary control bus, a PRECHARGE command on the first memory bank.

37.	A memory comprising:

an interface that is configured to communicate with a supplementary control bus, wherein the supplementary control bus comprises: a supplementary chip select bus, and a supplementary·bank select bus;

wherein activation of the supplementary chip select bus causes execution of a PRECHARGE command on a first memory bank that is identified by signals on the supplementary chip select bus and the supplementary bank select bus.

38.	A memory device according to claim 37 further comprising an interface that is configured to communicate with a main control bus, wherein the main control bus is configured to assert at least one of ACTIVE, READ and WRITE commands in conjunction with an address bus.

39.	A memory device according to claim 38 wherein the memory device is configured to assert an ACTIVE command, via the main control bus, on a second memory bank, and wherein the memory device is further configured to concurrently assert, via the supplementary control bus, a PRECHARGE command on the first memory bank.

40. A method for accessing a memory comprising the steps of:

asserting a first signal on a supplementary chip select bus, wherein assertion of the first

signal on the supplementary chip select bus executes a supplementary command on a first

memory bank, wherein the first memory bank is designated by the first signal on the

supplementary chip select bus and a second signal on a supplementary bank select bus;

and

asserting, via a main command bus, a main command on the first memory bank.

41. The method of claim 40 further comprising the steps of:

asserting, via a main command bus, one of a READ command and a WRITE command

on the first memory bank, wherein the one of said READ command and WRITE

command are asserted in association with an address communicated via an address bus.

42. The method of claim 41 further comprising the steps of:

asserting, via said main command bus, the main command on a second memory bank

concurrently with assertion, via the supplementary chip select bus, of the supplementary

command on the first memory bank.

43. The method of claim 42 wherein the supplementary command comprises one of a

PRECHARGE and PRE-ACCESS command.

44. The method of claim 42 wherein the main command comprises an ACTIVE command.

45. A method for accessing a memory comprising the steps of:

asserting a signal on a supplementary command bus, wherein assertion of the signal on

the supplementary command bus executes a supplementary command on a first memory

bank; and

asserting, via a main command bus, a main command on the first memory bank.

46. The method of claim 45 further comprising the steps of:

asserting, via a main command bus, one of a READ command and a WRITE command on the first memory bank, wherein said one of the READ command and WRITE command are asserted in association with an address communicated via an address bus.

47. The method of claim 45 further comprising the steps of:

asserting, via the main command bus, the main command on a second memory bank; and

concurrently asserting, via the supplementary control bus, a PRECHARGE command on said first memory bank.

48. The method of claim 47 wherein the supplementary command comprises one of a PRECHARGE and PRE-ACCESS command.

49. The method of claim 47 wherein the main command comprises an ACTIVE command.

50. A method for accessing a memory comprising the steps of:

activating rows and select columns for memory access operations using a main control bus; and

closing banks of memory using a supplementary control bus.

51. The method of claim 50 wherein the activating step further comprises the steps of:

identifying a first memory location on a first memory bank based on first signals from a main bank select bus, a main chip select bus, and an address bus;

providing an ACTIVE signal, on the main command bus, at a first time;

identifying a second memory location on a second memory bank, wherein the second memory location is identified by second signals from the main chip select bus, main bank select bus, and address bus; and

providing one of a READ command and a WRITE command to the second memory

location at a second time.

52.   The method of claim 51 further comprising the step of providing a supplementary

command, on a supplementary command bus, to the first memory bank at the second time.

53.   The method of claim 52 wherein the supplementary command is a PRECHARGE

command and wherein the PRECHARGE command closes a still-active row from the preceding

memory access operation.

54.   The method of claim 52 wherein said supplementary command comprises a NOP

command, delivered via a supplementary control bus at the first time.

55.   The method of claim 52, wherein said supplementary command comprises one of the

following commands: DESELECT, NO OPERATION, BURST TERMINATE, PRECHARGE,

AUTO REFRESH, and LOAD MODE REGISTER.

56.   A method for accessing a memory comprising the steps of:

asserting a first signal on a supplementary command bus, wherein assertion of the first

signal on the supplementary command bus executes a supplementary command on a first

memory bank, wherein the step of asserting the first signal on the supplementary

command bus further comprises packetizing of the supplementary command; and

asserting, via a main command bus, a main command on the first memory bank.

57.   The method of claim 56, wherein the step of packetizing comprises sending consecutive

signals for a single, lower priority command, and wherein the supplementary control bus is

configured with two supplementary command bits, a supplementary chip select bit, and

supplementary bank select bit.

58.   The method of claim 57, wherein the supplementary command bus is configured to receive at least one of executable commands PRECHARGE, AUTO REFRESH, and NOP, and secondary command indicator EXTEND1, wherein EXTEND1 designates a secondary command to be performed in a subsequent cycle, and wherein upon assertion of EXTEND1, the next cycle contains the secondary command.

59.   The method of claim 58 wherein EXTEND1 comprises one of: SELF REFRESH, WAKE, and LOAD MODE.

60.   The method of claim 58, wherein the secondary command is a command that is lower in priority than the main commands.

61.   The method of claim 56 further comprising the steps of:

asserting, via a main command bus, one of a READ command and a WRITE command on the first memory bank, wherein said one of the READ command and WRITE command are asserted in association with an address communicated via an address bus;

asserting, via said main command bus, the main command on a second memory bank; and

concurrently asserting, via the supplementary command bus, a PRECHARGE command on said first memory bank.

62.   The method of claim 59 wherein the supplementary command comprises one of a PRECHARGE and PRE-ACCESS command.

63.   The method of claim 59 wherein the main command comprises an ACTIVE command.

64.   The method of claim 58 further comprising the steps of:

asserting a tertiary command.

65.   The method of claim 64, wherein the secondary command is a tertiary command

indicator, and wherein the tertiary command indicator indicates another command following, in a

subsequent cycle, and wherein a tertiary command is asserted in the following cycle.